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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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TOLER & LARSON & ABEL, L.L.P.
5000 PLAZA ON THE LAKE
SUITE 265
AUSTIN, TX 78746

EXAMINER	
CHEN, SHIN HON	

ART UNIT	PAPER NUMBER
2131	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,308	DUCHARME, PAUL	
	Examiner	Art Unit	
	Shin-Hon Chen	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-40 have been examined.

Specification

Content of Specification

(a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of the specification unless the title is provided in an application data sheet. The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters.

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

(c) Statement Regarding Federally Sponsored Research and Development: See MPEP § 310.

(d) The Names Of The Parties To A Joint Research Agreement: See 37 CFR 1.71(g).

(e) Incorporation-By-Reference Of Material Submitted On a Compact Disc: The specification is required to include an incorporation-by-reference of electronic documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were permitted as electronic documents on compact discs beginning on September 8, 2000.

Or alternatively, Reference to a "Microfiche Appendix": See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.

(f) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

(g) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

(h) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.

(i) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or readily available publication which adequately describes the subject matter.

(j) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(k) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the

international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

(l) Sequence Listing, See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

2. Summary of the invention is missing. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6, 8-10, 13, 14, and 33-36 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Easter et al. U.S. Pat. No. 5563950 (hereinafter Easter).

5. As per claim 1, Easter discloses monolithic semiconductor device comprising: a first encryption engine having an input port (Easter: figure 2 and column 4 lines 50-56); a memory location having an output port coupled to the input port, wherein a data value to be stored in said memory location is observable only internally to the monolithic semiconductor device (Easter: figure 2 and column 4 lines 49-65 and column 2 lines 62-64).

6. As per claim 2, Easter discloses the monolithic semiconductor device as in claim 1. Easter further discloses wherein said memory location is observable only to said first encryption engine (Easter: figure 2 and column 4 lines 50-65).

7. As per claim 3, Easter discloses the monolithic semiconductor device as in claim 1. Easter further discloses said memory location is to store an encryption key (Easter: figure 2 and column 4 line 57 – column 5 line 11).

8. As per claim 4, Easter discloses the monolithic semiconductor device as in claim 1. Easter further discloses wherein said memory location includes a register (Easter: figure 2).

9. As per claim 5, Easter discloses the monolithic semiconductor device as in claim 1. Easter further discloses wherein said memory location includes non-volatile memory (Easter: column 4 lines 57-65).

10. As per claim 6, Easter discloses the monolithic semiconductor device as in claim 5. Easter further discloses wherein a value stored in said memory location is defined during a manufacture of the monolithic semiconductor device (Easter: column 3 lines 54-64).

11. As per claim 8, Easter discloses the monolithic semiconductor device as in claim 6. Easter further discloses wherein the value is defined using a laser etching technique (Easter: column 6 lines 5-13).

12. As per claim 9, Easter discloses the monolithic semiconductor device as in claim 1. Easter further discloses wherein said memory location includes volatile memory (Easter: column 4 lines 57-65).

13. As per claim 10, Easter discloses the monolithic semiconductor device as in claim 9. Easter further discloses wherein a value stored in said memory location is provided by said first encryption engine (Easter: figure 2 and column 4 lines 54-56).

14. As per claim 13, Easter discloses the monolithic semiconductor device as in claim 1. Easter further discloses the device comprising: at least one silicon die pad having an input coupled to the output of said memory location to provide a temporary access to said memory location (Easter: figure 2 and column 4 lines 50-65).

15. As per claim 14, Easter discloses the monolithic semiconductor device as in claim 1. Easter further discloses the device comprising an unique ID register coupled to the input of said encryption engine to store an unique ID (Easter: column 5 lines 27-36 and figure 3).

16. As per claim 33, Easter discloses a method comprising the steps of: accessing, by an encryption engine internal to a monolithic semiconductor device, data from a memory location internal to the monolithic semiconductor device, wherein the memory location is accessible only internal to the monolithic semiconductor device; and performing an encryption function using the data (Easter: figure 2 and column 4 lines 49-65 and column 2 lines 62-64).

17. As per claim 34, Easter discloses the method as in claim 33. Easter further discloses wherein the data is accessible only by the encryption engine (Easter: figure 2).

18. As per claim 35, Easter discloses the method as in claim 33. Easter further discloses wherein the data represents an encryption key (Easter: figure 2).

19. As per claim 36, Easter discloses the method as in claim 35. Easter further discloses the method including the steps of: generating the encryption key; and providing the encryption key for storage in the memory location (Easter: figure 2 and column 4 lines 50-65).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Easter in view of Loh et al. U.S. Pub. No. 20030093661 (hereinafter Loh).

22. As per claim 7, Easter discloses the monolithic semiconductor device as in claim 6. Easter does not explicitly disclose wherein the value is defined using a lithographic technique. However, Loh discloses that limitation (Loh: [0003]:use of lithography). It would have been

obvious to one having ordinary skill in the art to define value of the memory location using lithographic technique because lithography is one of the most common technique for hardwired programming of the ROM on semiconductor. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's invention to combine the teachings of Loh within the system of Easter because lithography is well known technique in semiconductor industry.

23. Claims 11, 12, 17-19, 21-27, 30-32, and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Easter in view of Pitts U.S. Pub. No. 20020145931 (hereinafter Pitts).

24. As per claim 11, Easter discloses the monolithic semiconductor device as in claim 1. Easter further discloses the device comprising: an external port having an input and output (Easter: figure 2). Easter does not explicitly disclose an isolation portion coupled to the input of said external port and to the output of said memory location, wherein said isolation portion to prevent access to said memory location using said external port. However, Pitts discloses an isolation fuse element that enforces one time programming of the memory (Pitts: [0011]: the fuse element and figure 1:104). It would have been obvious to one having ordinary skill in the art at the time of applicant's invention to include a fuse element in the semiconductor device because semiconductor device with fuse is well known in the art. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's invention to combine the teachings of Pitts within the system of Easter because it prevents external access to the memory location after data has been successfully stored into secure memory array.

25. As per claim 12, Easter as modified discloses the monolithic semiconductor device as in claim 11. Easter as modified further discloses wherein said isolation portion includes a fuse coupled between the input of said external port and the output of said memory location (Pitts: Pitts: [0011]: the fuse element and figure 1:104).

26. As per claim 17, Easter discloses a monolithic semiconductor device comprising: an external data port having an input and an output; a first encryption engine having an input coupled to the input of said external data port and an output; a memory location having an output coupled to the input of said first encryption engine (Easter: figure 2 and column 4 lines 50-56). Easter does not explicitly disclose an isolation portion coupled to the output of said memory location and to the input of said external data port, wherein said isolation portion is modifiable to permanently prevent access of said memory location by the external data port. However, Pitts discloses an isolation fuse element that enforces one time programming of the memory (Pitts: [0011]: the fuse element and figure 1:104). It would have been obvious to one having ordinary skill in the art at the time of applicant's invention to include a fuse element in the semiconductor device because semiconductor device with fuse is well known in the art. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's invention to combine the teachings of Pitts within the system of Easter because it prevents external access to the memory location after data has been successfully stored into secure memory array.

27. As per claim 18, Easter as modified discloses the device as in claim 17. Easter further discloses wherein said memory location includes non-volatile memory (Easter: column 4 lines 57-65).

28. As per claim 19, Easter as modified discloses the device as in claim 18. Easter further discloses wherein a value stored in said memory location is defined during a manufacture of the monolithic semiconductor device (Easter: column 3 lines 54-64).

29. As per claim 21, Easter as modified discloses the device as in claim 19. Easter further discloses said value is defined using a laser etching technique (Easter: column 6 lines 5-13).

30. As per claim 22, Easter as modified discloses the device as in claim 17. Easter further discloses wherein said memory location includes volatile memory (Easter: column 4 lines 57-65).

31. As per claim 23, Easter as modified discloses the device as in claim 22. Easter further discloses wherein a value stored in said memory location is provided by said first encryption engine (Easter: figure 2 and column 4 lines 54-56).

32. As per claim 24, Easter as modified discloses the device as in claim 17. Easter further discloses wherein sad memory location is located in a specific location of the monolithic semiconductor device (Easter: figure 2).

33. As per claim 25, Easter as modified discloses the device as in claim 17. Easter further discloses wherein said memory location is to store an encryption key (Easter: figure 2 and column 4 lines 50-65).

34. As per claim 26, Easter as modified discloses the device as in claim 25. Easter further discloses wherein said memory location is to store a plurality of encryption keys (Easter: figure 2 and column 4 lines 50-65).

35. As per claim 27, Easter as modified discloses the device as in claim 25. Easter further discloses wherein said encryption engine is to use a portion of the encryption key to perform an encryption function (Easter: figure 2 and column 4 lines 50-65).

36. As per claim 30, Easter as modified discloses the device as in claim 17. Easter as modified further discloses wherein said isolation portion includes a fuse coupled between the input of said external port and the output of said memory location (Pitts: Pitts: [0011]: the fuse element and figure 1: 104).

37. As per claim 31, Easter as modified discloses the device as in claim 17. Easter as modified further discloses the device comprising: at least one silicon die pad having an input coupled to the output of said memory location to provide a temporary access to said memory location (Easter: figure 2 and column 4 lines 50-65).

38. As per claim 32, Easter as modified discloses the monolithic semiconductor device as in claim 1. Easter further discloses the device comprising an unique ID register coupled to the input of said encryption engine to store an unique ID (Easter: column 5 lines 27-36 and figure 3).

39. As per claim 37, Easter discloses the method as in claim 33. Easter does not explicitly disclose the method including the steps of: accessing externally the data from the memory location; and isolating the memory location from subsequent external access. However, Pitts discloses an isolation fuse element that enforces one time programming of the memory (Pitts: [0011]: the fuse element and figure 1:104). It would have been obvious to one having ordinary skill in the art at the time of applicant's invention to include a fuse element in the semiconductor device because semiconductor device with fuse is well known in the art. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's invention to combine the teachings of Pitts within the system of Easter because it prevents external access to the memory location after data has been successfully stored into secure memory array.

40. As per claim 38, Easter as modified discloses the method as in claim 37. Easter as modified further discloses the step of accessing externally includes verifying a value of the data (Pitts: [0011]: allow loading and testing of the secure memory array).

41. As per claim 39, Easter as modified discloses the method as in claim 37. Easter as modified further discloses the step of accessing externally includes defining a value of the data (Pitts: [0011]).

42. As per claim 40, Easter as modified discloses the method as in claim 37. Easter as modified further discloses the step of isolating includes blowing a fuse which allows external access to the memory location (Pitts: [0011]).

43. Claims 15, 16, 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Easter in view of Van Oorschot et al. U.S. Pat. No. 5850443 (hereinafter Van Oorschot).

44. As per claim 15, Easter discloses the monolithic semiconductor device as in claim 1. Easter does not explicitly disclose a second encryption engine having an input coupled to the output port of said first encryption engine, and wherein said first encryption engine is a asymmetrical encryption engine and said second encryption is a symmetrical encryption engine. However, Van Oorschot discloses that limitation (Van Oorschot: column 5 lines 39-59). It would have been obvious to one having ordinary skill in the art to include second encryption engine into the semiconductor device because multiple encryption engines can be applied by different cryptographic operations. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's invention to combine the teachings of Van Oorschot within the system of Easter because it provides multiple layers of encryption/decryption to secure data being transferred.

45. As per claim 16, Easter as modified discloses the monolithic semiconductor device as in claim 15. Easter as modified further discloses wherein said first encryption engine is to provide a symmetrical encryption key to said second encryption engine, and wherein said second encryption key is to perform an encryption function using the symmetrical encryption key (Van Oorschot: column 5 lines 39-59).

46. As per claim 28, Easter as modified discloses the device as in claim 25. Easter as modified does not explicitly disclose the device including a second encryption engine having an input coupled to the output port of said first encryption engine, and wherein said first encryption engine is an asymmetrical encryption engine and said second encryption engine is a symmetrical encryption engine. However, Van Oorschot discloses that limitation (Van Oorschot: column 5 lines 39-59). It would have been obvious to one having ordinary skill in the art to include second encryption engine into the semiconductor device because multiple encryption engines can be applied by different cryptographic operations. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's invention to combine the teachings of Van Oorschot within the combination of Easter-Pitts because it provides multiple layers of encryption/decryption to secure data being transferred.

47. As per claim 29, Easter as modified discloses the device as in claim 28. Easter as modified further discloses wherein said first encryption engine is to provide a symmetrical encryption key to said second encryption engine, and wherein said second encryption key is to

perform an encryption function using the symmetrical encryption key (Van Oorschot: column 5 lines 39-59).

48. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Easter in view of Pitts and further in view of Loh.

49. As per claim 20, Easter as modified discloses the device as in claim 19. Easter as modified does not explicitly disclose wherein said value is defined using a lithographic technique. However, Loh discloses that limitation (Loh: [0003]:use of lithography). It would have been obvious to one having ordinary skill in the art to define value of the memory location using lithographic technique because lithography is one of the most common technique for hardwired programming of the ROM on semiconductor. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's invention to combine the teachings of Loh within the combination of Easter-Pitts because lithography is well known technique in semiconductor industry.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shin-Hon Chen whose telephone number is (571) 272-3789. The examiner can normally be reached on Monday through Friday 8:30am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shin-Hon Chen
Examiner
Art Unit 2131

SC

AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100